32.8 A Passive UHF RFID Transponder for EPC Gen 2 with -14dBm Sensitivity in 0.13µm CMOS

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The acceptance of the EPC Class 1 Generation 2 standard by the supply management community has opened up the way for Radio Frequency Identification suppliers to provide solutions with complete interoperability [1]. The Gen 2 standard offers advantages over preceding standards such as increased throughput and superior operation in dense reader environments [2]. The key performance driven component of the UHF RFID system is the RFID transponder or tag, consisting of a Transponder System on Chip (TSoC) mounted with a low cost printed dipole antenna in a label-like fashion. Several passive RFID transponders have been published in the literature [2-4] with various sensitivities; however, each has used a much simpler protocol than that required by the EPC Gen 2 specification. The more complex Gen 2 protocol is required by the marketplace, so as to combat numerous non-ideal issues that occur while communicating with thousands of tags using single or multiple readers. Implementing a more complex protocol requires additional processing power and places a higher burden on the TSoC when it comes to sensitivity, which ultimately leads to maximum read distance. An EPC Gen 2 compliant TSoC is described containing RF, nano-power analog, EEPROM and digital circuitry fabricated in 0.13µm CMOS. The IC supports an 860 to 960MHz carrier frequency with receive data rates from 40 to 160kb/s and achieves a -14dBm sensitivity. The main functions included are: i) Vdd generation & excess power handling, ii) data detection & transmission, iii) non-volatile memory and control and, iv) digital processing to implement the communication protocol. Figure 32.8.1 shows a simplified block diagram of the TSoC illustrating the RF, analog and digital components.

The chip derives its power supply by rectification of the input RF signal into a DC voltage by a multi-stage rectifier that utilizes a custom no mask added Schottky diode [5]. The voltage is regulated down progressively to a value of Vdd=1.45V using the rectifier, DC limiter and voltage regulator combination denoted by “A”. The RF limiter, denoted by “B”, ensures that the under large RF power levels, the voltage swing at the chip input is limited to 1.8V. Details of the Vdd generation and regulation are shown in Fig. 32.8.2.

The output of the rectifier (V_REC) is connected to a DC limiter, consisting primarily of D0, D1 and M0. The DC limiter provides a bypass path for excess current from the rectifier and hence prevents large voltages from occurring when the impinging RF power is high. The DC limiter kicks in significantly only when the voltage, V_REC, is above 1.4V. Hence, it does not waste current when the RF levels are low and the voltages are low.

R1-R6, M1-M6 along with R0 help shape the DC limiter’s I-V curve, so that the output of the limiter (V_LIM) is as flat as possible, as the rectifier current increases beyond a certain value. Meanwhile, the Schottky diodes S0 and S1 prevent reverse leakage from the load cap C_L into the limiter during a period of no RF. A simplified schematic of the fine regulator is shown in Fig. 32.8.2 and regulates Vdd when V_LIM > 1.45V. At low RF levels, when V_LIM < 1.45V, the feedback loop rails and pass device, Mp, acts as a switch making Vdd=V_LIM. Md1 and Rd1 provide extra bias to the amplifier during times of availability of extra RF power. This improves the bandwidth of the regulator. Additional details on the rectifier and power management can be found in [5] and [6].

Figure 32.8.1 block “C” denotes the RF demodulator circuitry. The envelope of the RF signal contains the data, and an envelope detector that is similar to the first stage of the rectifier is used as the demodulator. Figure 32.8.3 shows details of the demodulator and data detector. R_{dec} and C_{dec} set the decay time constant of the envelope detector. The block labeled “C” provides non-linear attenuation of the envelope based on the gate voltage of the RF limiter transistor shown in block “A”. This ensures the demodulated envelope voltage (V_{dem}) does not exceed the input range of the comparator.

The block labeled “D” passes the demodulated voltage of the envelope (V_{dem}) and generates a slightly scaled down average (V_{avg}) of this value. The two voltages are compared and the difference voltage is resolved to logic levels using a latch, clocked by a free-running on-chip oscillator at 1.28MHz. This over-sampled single bit data stream is recovered by the subsequent digital clock and data recovery circuit that includes a pulse interval encoder for the data detection. For the transmission of data back to the reader, M0 in Fig. 32.8.1 is used as a backscatter device. M0 acts to mismatch the IC impedance with the antenna, thereby reflecting the incident power and signaling a data “high”. The circuits previously discussed perform the major AFE functions relating to Vdd generation, data reception and transmission. Another key function of the TSoC is the random number generator.

The required anti-collision protocol implemented in the chip requires random number generation. The random number generator on the IC is a unique combination of an Analog Random Number Generator (ARNG) and a digital Pseudo Random Number Generator (PRNG). The PRNG is implemented using standard techniques however the ARNG is implemented using a new method. This is done by sampling the RF carrier signal using a jittery clock and is illustrated in Fig. 32.8.4. In this schematic, the signal at “A” is the coupled fixed carrier frequency centered about RF_gnd. The input sampling NMOS devices are driven using a clock labeled “samp” and the RMS jitter of the clock is 8 times the period of the RF sinusoid. This ensures that there is an equal chance of sampling the RF when it is above or below ground. Samples taken using a 1.28MHz jittery clock provide a random number bit stream that is collected and used in conjunction with the PRNG to produce a final 16b random number. The advantage of using this technique is that it provides a true random number with a power consumption of only a few hundred nanowatts. Meanwhile, additional important functions of the TSoC are illustrated in Fig. 32.8.1 including EEPROM programming circuits and the system power on reset (POR).

Measurement data was taken through a variety of methods, including on-chip wafer probing with RF injection probes, as well as with completely assembled tags through a controlled air interface. Figure 32.8.5 shows a receive data command and the transmission or response via backscatter communication using a wafer probe injection and collection setup. The internal backscatter signal is also captured through on-chip probing of the device as shown at the bottom of the figure. A summary of the performance of a completely assembled RFID tag is given in Fig. 32.8.6. Testing of the device was performed with several readers from various vendors exercising the range of the EPC Gen 2 specification. A micrograph of the 0.55mm^2 die is shown in Fig. 32.8.7.

Acknowledgements:
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References:
[1] EPC Class 1 Generation 2 UHF Air Interface Protocol Standard Version 1.0.9
[2] R. Glidden, et al., “Design of Ultra-Low-Cost UHF RFID Tags for Supply Chain Applications,” *IEEE Communications Magazine*, vol. 42, pp. 140-151, Aug., 2004.
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[6] G. Balachandran, and R. Barnett, “A 110nA Voltage Regulator System With Dynamic Bandwidth Boosting for RFID Systems,” *IEEE J. Solid-State Circuits*, vol. 41, pp. 2019-2028, Sept., 2006.

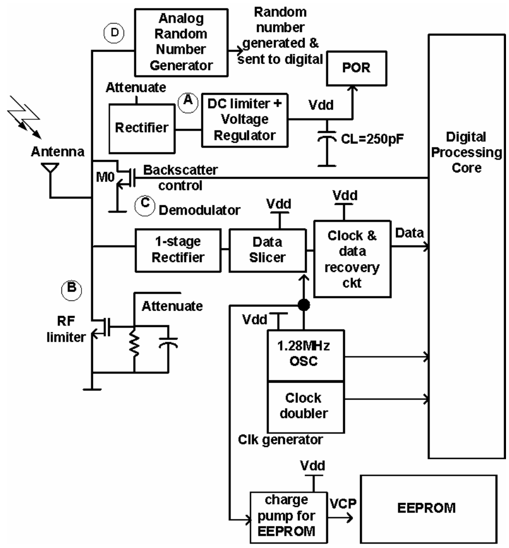

Figure 32.8.1: Block diagram of the Transponder SoC.

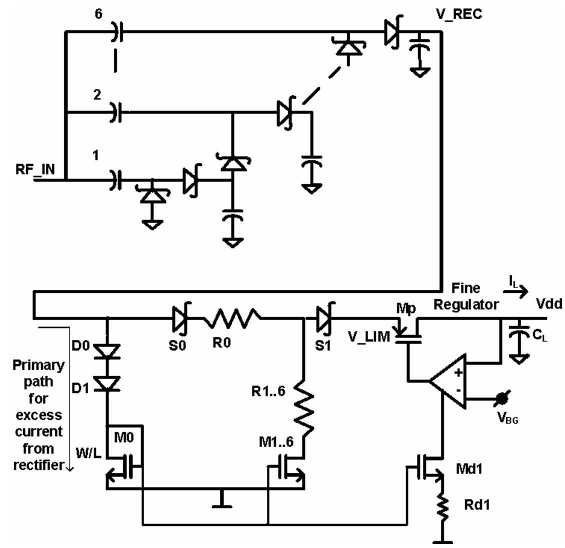

Figure 32.8.2: Vdd generation and regulation.

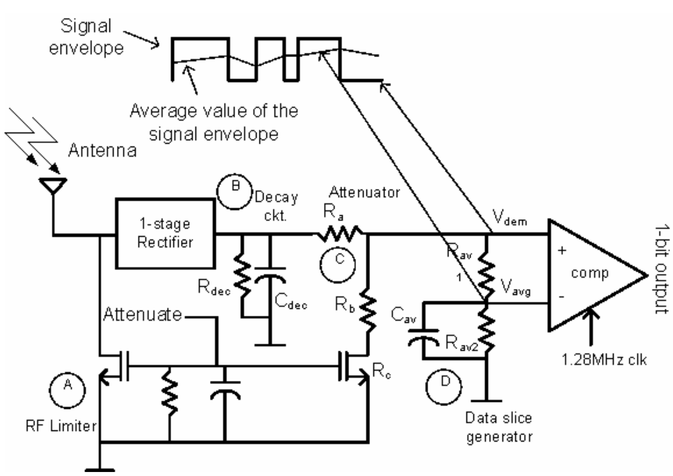

Figure 32.8.3: Data detector simplified schematic.

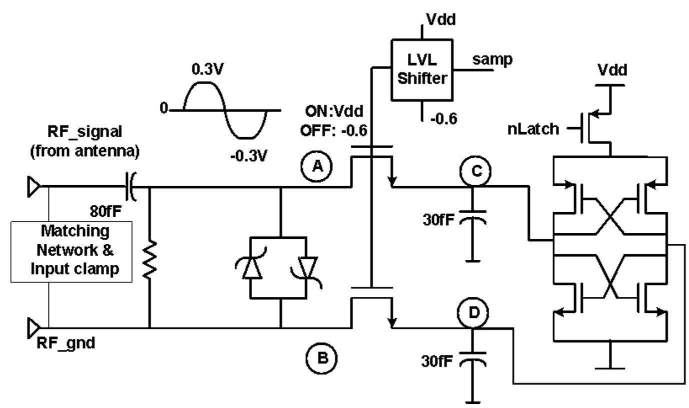

Figure 32.8.4: RF sampling Analog Random Number Generator.

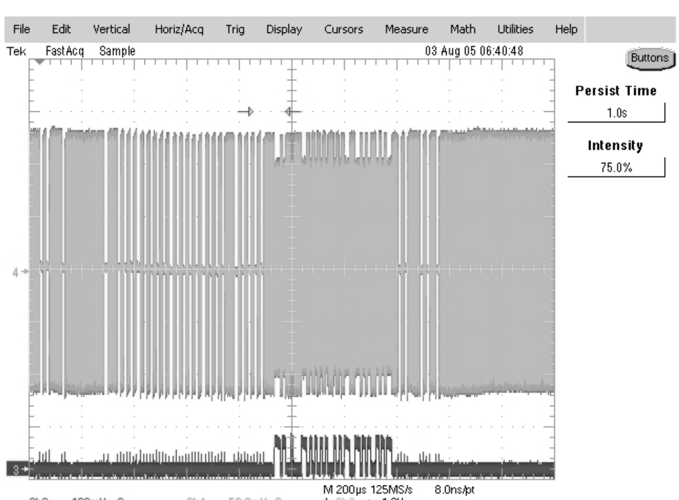

Figure 32.8.5: Receive data command and backscatter response.

Technology	130nm CMOS with EEPROM and no mask added Schottky diode
Carrier Frequency	860-960MHz
RX Data Rate	40-160kb/s
TX Data Rate	40-640kb/s
Modulation Format	ASK PR-ASK
Typical Sensitivity	-14dBm
User non-volatile memory	192b
Typical Working Distance	7 meters
Commands Supported	EPCglobal Class 1 Gen 2 Compliant
Die Area	$0.55mm^2$

Figure 32.8.6: Performance summary for the TSoC.

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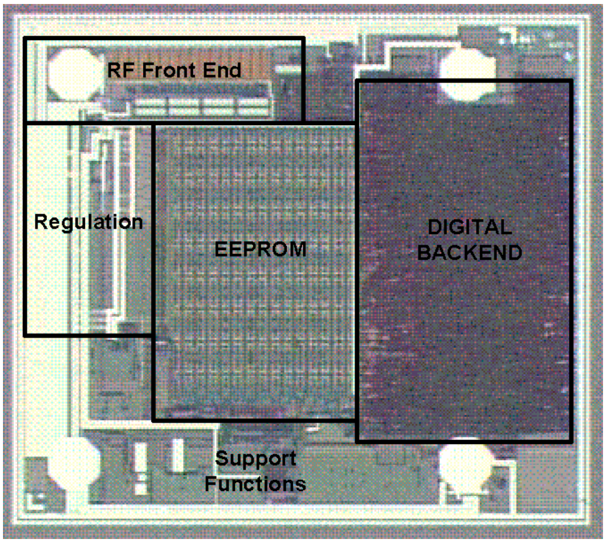

Figure 32.8.7: Die micrograph.